10/27/99 JC685 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	970901A	Total Pages	
	First Named Inventor or Application Identifier			
	Kiyoshi IRINO			
	Express Mail Label No.			
Check Box, if applicable [ ] Duplicate	PAGE 1 OF 3			

JC675 U.S. PTO 09/428052 10/27/99

APPLICATION ELEMENTS FOR:	ADDRESS TO:
METHOD OF FABRICATING A SEMICONDUCTOR DEVICE CONTAINING NITROGEN IN A GATE OXIDE FILM (As Amended)	Assistant Commissioner for Patents BOX PATENT APPLICATIONS Washington, D.C. 20231

1. [X] Fee Transmittal Form (Incorporated within this form)
   (Submit an original and a duplicate for fee processing)

2. [X] Specification — Total Pages [23]

3. [X] Drawing(s) (35 USC 113) — Total Sheets [12]

4. [X] Oath or Declaration — Total Pages [2]

   a. [ ] Newly executed (original or copy)

   b. [X] Copy from prior application (37 CFR 1.63(d) (for continuation/divisional with Box 17 completed).

      i. [ ] Deletion of Inventor(s)
      Signed statement attached deleting inventor(s) named in prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [X] Incorporation by reference (usable if box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement Verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet and document(s)) (copy from prior application)

9. [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [ ] Power of Attorney

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	970901A
	First Named Inventor or Application Identifier	
	Kiyoshi IRINO	
	PAGE 2 OF 3	

10. [ ] English translation Document (if applicable)
11. [X] Information Disclosure Statement [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired.
15. [X] Claim for Convention Priority [ ] Certified copy of Priority Document(s)
    a. Priority of Japan application no.9-052085, filed on March 6, 1997 is claimed under 35 USC 119. The certified copies have been filed in prior application Serial No. 08/917,936. (For Continuing Applications, if applicable).
16. [ ] Other ______________________________
17. [X] If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

    [ ] Continuation [X] Division [ ] Continuation-in-part (CIP) of prior application no. 08/917,936

    a. [X] Please amend the specification by inserting after the title: --This application is a divisional of prior application Serial No. 08/917,936, filed August 27, 1997--.

    b. [X] Cancel in this application original claims 1 - 5 and 14 of the prior application before calculating the filing fee.

FEE TRANSMITTAL The filing fee is calculated below	Number Filed	Number Extra	Rate	Basic Fee $760.00
Total Claims	8 - 20	0	x $18.00	
Independent Claims	2 - 3	0	x $78.00	
Multiple Dependent Claims			$260.00	
			Basic Filing Fee	$760.00
Reduction by 1/2 for small entity				
Fee for recording enclosed Assignment			$40.00	
TOTAL				$760.00

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	970901A
	First Named Inventor or Application Identifier	
	Kiyosi IRINO	
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[X] A check in the amount of $760.00 is enclosed to cover the filing fee.

[ ] Please charge our Deposit Account No. **01-2340** in the total amount of $ to cover the filing fee and the $ assignment recordation fee. A duplicate of this sheet is attached.

[X] The Commissioner is hereby authorized to charge payment for any additional filing fees required under 37 CFR 1.16 or credit any overpayment to Deposit Account No. **01-2340**. A duplicate of this sheet is attached.

18. CORRESPONDENCE ADDRESS

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SUBMITTED BY	
Typed or Printed Name Stephen G. Adrian	Reg. No. 32,878
Signature	Date: October 27, 1999

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: kiyoshi IRINO

Serial No.: Divisional of SN 08/917,936 — Art Unit: Not Yet Assigned

Filed: Herewith — Examiner: Not Yet Assigned

For: METHOD OF FABRICATING A SEMICONDUCTOR DEVICE CONTAINING NITROGEN IN A GATE OXIDE FILM (As Amended)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

October 27, 1999

Sir:

Prior to examination on the merits, please amend the above-identified application as follows:

IN THE TITLE:

Please amend the title to read:

--METHOD OF FABRICATING A SEMICONDUCTOR DEVICE CONTAINING NITROGEN IN A GATE OXIDE FILM--.

IN THE CLAIMS:

Please cancel claims 1-5 and 14.

REMARKS

Claims 6-13 are pending. The above amendments are believed to place the application in better condition for examination.

Prompt and favorable action on the merits is earnestly solicited.

In the event any fees are required in connection with this paper, please charge Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON

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Reg. No. 32,878

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SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT I, Kiyoshi Irino, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan have invented certain new and useful improvements in

SEMICONDUCTOR MEMORY DEVICE CONTAINING NITROGEN IN A GATE OXIDE FILM

of which the following is a specification : -

TITLE OF THE INVENTION

SEMICONDUCTOR MEMORY DEVICE CONTAINING NITROGEN IN A GATE OXIDE FILM

BACKGROUND OF THE INVENTION

The present invention generally relates to fabrication of semiconductor devices and more particularly to fabrication and construction of a high speed field-effect transistor.

High-speed logic integrated circuits generally use high-speed CMOS circuits. CMOS circuits consume little electric power and are particularly suited for this purpose. In order to increase the operational speed of high-speed CMOS circuits further, a very fast field-effect transistor is needed.

Conventionally, the operational speed of a field-effect transistor has been increased mainly by reducing the gate length, which in turn is achieved by a device miniaturization. For example, MOS transistors having a gate length as small as 0.35 μm, are used these days for such high performance applications.

On the other hand, further reduction of gate length is generally difficult in MOS transistors, as carriers tend to experience excessive acceleration in a channel region immediately under a gate electrode of the MOS transistor when the gate length of the MOS transistor is thus reduced. The carriers thus accelerated tend to penetrate into a gate oxide film and form fixed electric charges therein, while such fixed electric charges tend to modify the threshold characteristics of the MOS transistor.

In more detail, the carriers thus penetrated into the gate oxide film enter the SiO_2 structure that form the gate oxide film, wherein the carriers thus penetrated into the SiO_2 structure are held stably when the carriers are captured by the dangling bonds

of the SiO_2 structure.

Thus, it has been practiced conventionally in the art of MOS transistors to terminate any dangling bonds existing in the gate oxide film by introducing N atoms thereinto, so that the number of the sites which may capture the carriers is reduced as much as possible.

FIGS.1A - 1D show a conventional fabrication process of a MOS transistor.

Referring to FIG.1A, a field oxide film 2 is formed on a Si substrate 1 doped to the p-type or n-type, such that the field oxide film 2 defines a device region 1A on the surface of the substrate 1. The field oxide film 2 is typically formed by a wet etching process with a thickness of 300 - 400 nm. Further, a thermal oxide film 3 is formed on the Si substrate 1 so as to cover the device region 1A with a thickness of typically about 6 nm. The thermal oxide film 3 acts as a gate oxide film of the MOS transistor to be formed.

The structure of FIG.1A is then annealed in an N_2O atmosphere at a temperature of typically 800°C, such that N atoms in the atmosphere are incorporated into the gate oxide film 3.

Next, in the step of FIG.1B, a polysilicon film 4 is deposited on the structure of FIG.1A by a CVD process conducted at a temperature of 800 - 900°C, typically with a thickness of about 150 nm. Further, the polysilicon film 4 is patterned in the step of FIG.1C by an anisotropic etching process such as an RIE (reactive ion etching) process, and a gate electrode 4A is formed as a result.

After the gate electrode 4A is thus formed, an ion implantation process of a p-type dopant such as B or an n-type dopant such as As or P is introduced into the substrate 1 while using the gate electrode 4A as a mask. Thereby, diffusion regions 1B and 1C are

formed in the substrate 1 respectively in correspondence to a source region and a drain region of the MOS transistor to be formed. Further, a CVD-SiO_2 film 5 is deposited on the structure thus obtained by a CVD process conducted at the temperature of 800 - 900°C, typically with a thickness of about 100 nm.

Next, in the step of FIG.1D, the CVD-SiO_2 film 5 is subjected to an anisotropic etching process that acts substantially vertically to the principal surface of the substrate 1, and side wall oxides 5A and 5B are formed at respective lateral sides of the gate electrode 4A. Further, by carrying out the ion implantation process of the p-type dopant or the n-type dopant once more into the substrate 1 in the state that the gate electrode 4A carries the side wall oxides 5A and 5B, further diffusion regions 1B' and 1C' having a higher dopant level are formed inside the diffusion regions 1B and 1C. In other words, the MOS transistor thus formed has a so-called LDD (lightly doped drain) structure.

It should be noted that, in the MOS transistor of the foregoing structure, the gate oxide film 3 acts as an etching stopper when patterning the gate electrode 4A. Thereby, the part of the gate oxide film 3 not protected by the gate electrode 4A may experience an increased degree of damage during the etching process. For example, the Si-O bonds in the SiO_2 structure of the gate oxide film 3 may be broken.

When such breaking of the Si-O bond occurs, dangling bonds are formed inevitably in the structure of the gate oxide film 3, while it is known that the dangling bonds tend to capture H or OH ions. In the case of the high speed MOS transistor of FIG.1D that has a short channel length, there is a substantial risk that the dangling bonds in the gate oxide film 3

capture the hot carriers that are accelerated at the edge of drain region 1C and penetrated into the gate oxide film 3 as indicated in FIG.2, wherein FIG.2 shows the drain region 1C in an enlarged scale.

In order to overcome the problem, it has been proposed to introduce N atoms into the gate oxide film 3 in the process of FIG.1A, such that the N atoms thus introduced terminate the dangling bonds in the gate oxide film 3. As a result of such a process, the trapping of the hot electrons by the dangling bonds is reduced substantially.

On the other hand, the conventional process of FIGS.1A - 1D raises a problem in that, because the N atoms are introduced at a relatively early phase of the process, the N atoms thus incorporated easily escape in the following processes, particularly those including thermal annealing processes. In other words, it has been necessary in the conventional process of FIGS.1A - 1D to incorporate a very large amount of N atoms into the gate oxide film 3 in order that such a doping by the N atoms is effective for suppressing the trapping of the hot carriers by the dangling bonds.

When the N atoms are introduced in the step of FIG.1A, it should be noted that the N atoms are introduced not only into the part of the gate oxide film 3 corresponding to the edge part of the drain region as shown in FIG.2 but also into the part immediately underneath the gate electrode 4A. Thereby, the MOS transistor thus obtained tends to show a threshold characteristic substantially different from the desired or designed threshold characteristic.

FIGS.3A and 3B show a flat-band voltage V_{FB} and a threshold voltage V_{TH} of the MOS transistor for the case in which the gate oxide film, formed as a result of a thermal oxidation process in a dry O_2

environment, is exposed to various N-containing atmospheres at a temperature of about 800°C.

Referring to FIGS.3A and 3B, it will be noted that both the V_{FB} and the V_{TH} are modified significantly as a result of the thermal annealing process conducted in the NO or N_2O atmospheres for various durations. As already noted, the concentration of the N atoms in the gate oxide film 3 is changed substantially by the heating processes included in the steps of FIGS.1A - 1D. Thus, it has been difficult in the conventional MOS transistor, fabricated according to the process of FIGS.1A - 1D, to control the characteristics thereof exactly, and there has been a problem in that the transistor shows a large scattering of the characteristics. This problem becomes particularly acute in the MOS transistors in which a very large amount of N atoms are introduced into the gate oxide film for effective termination of the dangling bonds therein.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful semiconductor device and a fabrication process thereof wherein the foregoing problems are eliminated.

Another and more specific object of the present invention is to provide a semiconductor device and a fabrication process thereof, wherein the problem of trapping of the hot carriers in the gate oxide film is successfully eliminated while simultaneously realizing a stable and reproducible device characteristic.

Another object of the present invention is to provide a semiconductor device, comprising:

a substrate;

a gate oxide film formed on said substrate;

a gate electrode provided on said gate oxide

film;

first and second diffusion regions formed in said substrate at both lateral sides of said gate electrode;

said gate electrode including a first region located immediately underneath said gate electrode and a second region adjacent to said first region, said first and second regions containing N atoms with respective concentrations such that said second region contains N with a higher concentration as compared with said first region.

According to the present invention, the variation of the threshold or other characteristic of the semiconductor device is successfully suppressed while simultaneously suppressing the problem of the trapping of the hot carriers in the gate oxide film in the vicinity of the drain edge.

Another object of the present invention is to provide a method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming a gate electrode pattern on said gate oxide film; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask.

According to the present invention, the N atoms are introduced into the gate oxide film selectively in correspondence to the edge part of the drain region where the acceleration of the carriers, and hence the formation of the hot carriers, is maximum, while the gate oxide film immediately underneath the gate electrode pattern is maintained substantially free form the N atoms. Thereby, the problem of trapping of the hot carriers in the gate oxide film is successfully avoided in the part where the creation of the hot carriers is maximum. As the

gate oxide film is substantially free from the N atoms in the part immediately underneath the gate electrode pattern, the designed operational characteristic is obtained for the semiconductor device with reliability and reproducibility.

Other objects and further features of the present invention will become apparent from the following detailed description when read in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS.1A - 1D are diagrams showing a conventional fabrication process of a semiconductor device;

FIG.2 is a diagram explaining the problem pertinent to the conventional semiconductor device;

FIGS.3A and 3B are further diagrams explaining the problem of the conventional semiconductor device;

FIG.4 is a diagram showing the principle of the present invention;

FIGS.5A - 5G are diagrams showing a fabrication process of a semiconductor device according to a first embodiment of the present invention;

FIG.6 is a diagram showing a distribution profile of N atoms in a gate oxide film of the semiconductor device of the first embodiment;

FIGS.7A - 7G are diagrams showing a fabrication process of a semiconductor device according to a second embodiment of the present invention; and

FIG.8 is a diagram showing the effect of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[PRINCIPLE]

FIG.4 shows the principle of the present invention, wherein those parts corresponding to the parts described previously are designated by the same reference numerals and the description thereof will be omitted.

Referring to FIG.4, the present invention introduces N atoms into a part of the gate oxide film 3 indicated by a hatched region selectively with respect to the adjacent region located immediately underneath the gate electrode pattern 4A. Thereby, it should be noted that the N atoms are contained mostly in the hatched region and the concentration of the N atoms in the adjacent region is held minimum. Thus, the problem of modification of the threshold characteristics of the semiconductor device by the N atoms thus doped into the gate oxide film 3 is effectively and successfully minimized.

In the construction of FIG.4, it should be noted that the N atoms are introduced selectively and with a high concentration level into the region that tends to experience most severe damages during the patterning process of the gate electrode pattern 4A. Further, the region of the gate oxide film 3 where the N atoms are introduced selectively corresponds to the part of the channel region where the creation of the hot carriers is maximum. Thus, any dangling bonds that are created as a result of the damage are immediately terminated by the N atoms and the problem of trapping of the hot carriers by the dangling bonds is successfully eliminated.

As the foregoing doping of the N atoms into the gate oxide film 3 is achieved after the deposition and patterning of the gate electrode pattern 4A, the problem of escaping of the N atoms by the heat caused during the deposition of the gate electrode pattern 4A is successfully avoided.

Further, when the doping of the N atoms is

conducted by exposing the gate oxide film 3 to the NO atmosphere, the subsequent process of depositing the side wall oxides 5A and 5B may be conducted immediately thereafter, in the same deposition apparatus, continuously and without exposing the substrate to the environment. It should be noted that the annealing process for introducing the N atoms is conducted at the temperature of about 800°C, while this temperature is the temperature used for depositing the side wall oxides 5A and 5B by way of a CVD process.

[FIRST EMBODIMENT]

FIGS.5A - 5G show the fabrication process of a MOS transistor according to a first embodiment of the present invention.

Referring to FIG.5A, a Si substrate 11 corresponding to the Si substrate 1 of FIG.1A is formed with a well 11a of the p-type or n-type, and a field oxide film 12 is formed on the substrate 11 by a wet oxidation process with a thickness of typically 300 - 400 nm, such that the field oxide film 12 defines a device region 11A on the surface of the substrate 11. Further, a thermal oxide film 13 is formed on the substrate 11 so as to cover the device region 11A with a thickness of typically 6 nm.

Further, in the step of FIG.5B, a polysilicon film 14 corresponding to the polysilicon film 4 of FIG.1B is deposited on the structure of FIG.5A typically with a thickness of about 15 nm by a CVD process conducted at a temperature of 800 - 900°C. The polysilicon film 14 thus formed is then subjected to an anisotropic etching process such as an RIE process in the step of FIG.5C and a gate electrode 14A is formed.

In the step of FIG.5C, a p-type dopant such as B or an n-type dopant such as As or P is further

introduced into the substrate 11 by an ion implantation process while using the gate electrode 14A as a mask, and diffusion regions 11B and 11C are formed in the substrate 11.

Further, the substrate 11 thus processed is introduced into a CVD apparatus and exposed to an atmosphere containing NO for a duration of typically 5 - 20 minutes. Because of the toxic nature of NO, it is preferable to use a diluted gas of NO for the foregoing exposure process in which NO is diluted in an Ar carrier gas with a volumetric concentration of about 30%. Further, it is desirable, for the sake of safety, to carry out the exposure under a reduced pressure environment of about 40 Pa, for example.

As a result of the thermal annealing applied during the exposure process, the impurity elements introduced previously by the ion implantation process cause a diffusion into the substrate 11 and the diffusion regions 11B and 11C noted previously are formed as a result of such a diffusion of the impurity element. Thus, the annealing process associated with an ion implantation process is achieved simultaneously to the thermal annealing process for introducing the N atoms in the present embodiment.

Next, in the step of FIG.5D, a CVD-SiO_2 film 15 is deposited on the structure of FIG.5C by a CVD process conducted in the same CVD apparatus at a temperature of typically about 800 °C, with a thickness of about 100 nm. It should be noted that the CVD process of FIG.5D is conducted continuously to the exposure process of FIG.5C.

Next, in the step of FIG.5E, the CVD-SiO_2 film 15 is subjected to an anisotropic etching process such as an RIE process acting substantially perpendicularly to the principal surface of the substrate 11, and side wall oxides 15A and 15B are formed at both lateral sides of the gate electrode

14A, similarly to the side wall oxides 5A and 5B of FIG.1D. Further, by conducting an ion implantation process of the foregoing p-type or n-type dopant into the substrate 11 in the state that the gate electrode 14A carry the side wall oxides 15A and 15B, an LDD structure including diffusion regions 11B' and 11C' having a higher impurity concentration level inside the diffusion regions 11B and 11C, are obtained.

Next, in the step of FIG.5F, an interlayer insulation film 16 of SiO_2 is deposited on the structure of FIG.5E with an appropriate thickness, and ohmic electrodes 17A and 17B are provided on the interlayer insulation film 16 in ohmic contact with the diffusion regions 11C and 11B respectively via contact holes formed in the interlayer insulation film 16.

In the present embodiment, the process of FIG.5C for introducing the N atoms into the gate oxide film 13 is carried out while using the gate electrode 14A as a mask. Thus, the incorporation of the N atoms does not occur in the part of the gate oxide film 13 located immediately underneath the gate electrode 14A and covering the channel region. Thus, no substantial change occurs in the threshold characteristic or flat-band characteristic of the MOS transistor even when the N atoms are introduced into the gate oxide film 13.

As the N atoms are introduced with a high concentration level selectively into the part of the gate oxide film 13 corresponding to the drain edge where the creation of the hot-carriers is most prominent, the dangling bonds in the SiO_2 structure forming the gate oxide film 13 are effectively terminated, and the sites for trapping hot-carriers are annihilated. Thus, the problem of trapping of the electrons or holes by the gate oxide film 13 is successfully avoided.

In the step of FIG.5C, it should be noted that the exposure process may be conducted in an atmosphere containing N_2O in place of NO. In this case, it is preferable to use the annealing temperature of about 900°C, rather than 800°C. Generally, the amount of the N atoms incorporated into the gate oxide film 13 is reduced when the exposure is carried out in the N_2O atmosphere rather than in the NO atmosphere. When N_2O is used in the step of FIG.5C, it is necessary to lower the temperature of the CVD apparatus to about 800 °C when carrying out the CVD process of FIG.5D. Such thermal annealing processes at different temperatures can be conducted efficiently by using a cluster-type processing apparatus.

FIG.6 shows the distribution profile of N atoms in the depth direction of the gate oxide film 13 as measured by a SIMS (secondary ion mass spectroscopy) analysis.

Referring to FIG.6, it should be noted that the concentration level of the N atoms is much higher when the thermal annealing process is conducted in the NO atmosphere rather than the case in which the thermal annealing process is conducted in the N_2O atmosphere. Further, FIG.6 indicates that the N atoms thus introduced are primarily concentrated in the vicinity of the interface between the gate oxide film 13 and the substrate 11. In other words, the N atoms introduced in the step of FIG.5C into the gate oxide film 13 tend to show a concentration to the interface to the substrate 11. It will be noted that the peak concentration level of the N atoms in the gate oxide film 13 is in the range of about 0.5% to about 2% or more.

In the present embodiment, the thermal annealing process of FIG.5C in the NO or N_2O atmosphere is carried out after the ion implantation

process for forming the diffusion regions 11B and 11C. This, however, is not a mandatory condition and it is also possible to carry out the thermal annealing process before the ion implantation process. In this case, however, it is necessary to carry out a separate thermal annealing process for activating the introduced impurity elements in the diffusion regions 11B and 11C.

[SECOND EMBODIMENT]

FIGS.7A - 7G show the fabrication process of a MOS transistor according to a second embodiment of the present invention.

Referring to FIG.7A, a Si substrate 21 corresponding to the Si substrate 1 of FIG.1A is formed with a well 21a of the p-type or n-type, and a field oxide film 22 is formed on the substrate 21 by a wet oxidation process with a thickness of typically 300 - 400 nm, such that the field oxide film 22 defines a device region 21A on the surface of the substrate 21. Further, a thermal oxide film 23 is formed on the substrate 21 so as to cover the device region 21A with a thickness of typically 6 nm.

Further, in the step of FIG.7B, a polysilicon film 24 corresponding to the polysilicon film 4 of FIG.1B is deposited on the structure of FIG.7A typically with a thickness of about 15 nm by a CVD process conducted at a temperature of 800 - 900°C. The polysilicon film 24 thus formed is then subjected to an anisotropic etching process such as an RIE process in the step of FIG.7C and a gate electrode 24A is formed.

In the step of FIG.7C, a p-type dopant such as B or an n-type dopant such as As or P is further introduced into the substrate 21 by an ion implantation process while using the gate electrode 24A as a mask, and diffusion regions 21B and 21C are

formed in the substrate 21.

In the step of FIG.7C, the substrate 21 thus processed is subjected to an ion implantation process in which N^+ ions are introduced into the gate oxide film 23 while using the gate electrode 24A as a mask. In the ion implantation process of N^+ atoms, the acceleration voltage is set such that the N^+ atoms do not reach the substrate 21. For example, the acceleration voltage is set to 100 keV or less, and the ion implantation may be made with a dose of 1 - 3 x $10^{14}cm^{-2}$ such that substantially the entire dangling bonds in the film 23 are terminated.

Next, in the step of FIG.7D, a CVD-SiO_2 film 25 is deposited on the structure of FIG.7C by a CVD process conducted in the same CVD apparatus at a temperature of typically about 800 °C, with a thickness of about 100 nm.

Next, in the step of FIG.7E, the CVD-SiO_2 film 25 is subjected to an anisotropic etching process such as an RIE process acting substantially perpendicularly to the principal surface of the substrate 21, and side wall oxides 25A and 25B are formed at both lateral sides of the gate electrode 24A, similarly to the side wall oxides 5A and 5B of FIG.1D. Further, by conducting an ion implantation process of the foregoing p-type or n-type dopant into the substrate 21 in the state that the gate electrode 24A carry the side wall oxides 25A and 25B, an LDD structure including diffusion regions 21B' and 21C' having a higher impurity concentration level inside the diffusion regions 21B and 21C, are obtained.

Next, in the step of FIG.7F, an interlayer insulation film 26 of SiO_2 is deposited on the structure of FIG.7E with an appropriate thickness, and ohmic electrodes 27A and 27B are provided on the interlayer insulation film 26 in ohmic contact with the diffusion regions 21C and 21B respectively via

contact holes formed in the interlayer insulation film 26.

In the present embodiment, too, the process of FIG.7C for introducing the N atoms into the gate oxide film 23 is carried out while using the gate electrode 24A as a mask. Thus, the incorporation of the N atoms does not occur in the part of the gate oxide film 23 located immediately underneath the gate electrode 24A and hence covering the channel region. Thus, no substantial change or modification occurs in the threshold characteristic or flat-band characteristic of the MOS transistor even when the N atoms are introduced into the gate oxide film 23.

As the N atoms are introduced with a high concentration level selectively into the part of the gate oxide film 23 corresponding to the drain edge where the creation of the hot-carriers is most prominent, the dangling bonds in the SiO_2 structure forming the gate oxide film 23 are effectively terminated, and the sites for trapping hot-carriers are annihilated. Thus, the problem of trapping of the electrons or holes by the gate oxide film 23 is successfully avoided.

FIG.8 shows, by a thick continuous line designated by "X," the degradation or variation ΔId of a drain current Id with a stress time, for a 64M bit DRAM that uses the MOS transistor of FIG.5G. Further, FIG.8 shows also a similar change of the drain current, by open circles and designated as "REF," for the case in which the MOS transistor is formed without incorporation of N atoms into the gate oxide film. Further, FIG.8 shows by solid circles the change of the drain current Id for the case in which the gate oxide film is annealed in an oxygen atmosphere. In any of the cases, the gate oxide film of the MOS transistor has a thickness of about 10 nm.

Referring to FIG.8, it should be noted that

the variation or degradation of the drain current ΔId with time is significantly suppressed by incorporating the N atoms into the gate oxide film excluding the region located immediately underneath the gate electrode.

Further, the present invention is not limited to the embodiments described heretofore, but various variations and modifications may be made without departing from the scope of the invention.

WHAT IS CLAIMED IS

1. A semiconductor device, comprising:

a substrate;

a gate oxide film formed on said substrate;

a gate electrode provided on said gate oxide film;

first and second diffusion regions respectively formed in said substrate at each lateral side of said gate electrode;

said gate electrode including a first region located right underneath said gate electrode and a second region adjacent to said first region, said first and second regions containing N atoms with respective concentrations such that said second region contains N with a higher concentration as compared with said first region.

2. A semiconductor device as claimed in claim 1, wherein said N atoms are distributed in said gate oxide film with a depth profile such that said depth profile has a peak in the vicinity of an interface between said gate oxide film and said substrate.

3. A semiconductor device as claimed in claim 1, wherein said gate oxide film contains said N atoms in said second region with a concentration level

of at least about 0.5%.

4. A semiconductor device as claimed in claim 1, wherein said gate oxide film contains said N atoms in said second region with a concentration level of at least about 1%.

5. A semiconductor device as claimed in claim 1, wherein said gate oxide film contains said N atoms in said second region with a concentration level of at least about 2%.

6. A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming a gate electrode pattern on said gate oxide film; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask.

7. A method as claimed in claim 6, wherein said step of introducing N atoms into said gate oxide film comprises a thermal annealing process of said gate oxide film conducted in an atmosphere containing

N atoms.

8. A method as claimed in claim 7, wherein said atmosphere contains NO and said thermal annealing process is conducted at a temperature of about 800°C.

9. A method as claimed in claim 9, wherein said atmosphere contains N_2O and said thermal annealing process is conducted at a temperature of about 900°C.

10. A method as claimed in claim 7, wherein asid step of introducing N atoms into said gate oxide film includes an ion implantation process of N ions.

11. A method as claimed in claim 10, wherein said ion implantation process is carried out under an acceleration voltage of not exceeding about 10 keV.

12. A method as claimed in claim 10, wherein said ion implantation process is carried out

with a dose of about $1 - 3 \times 10^{14} cm^{-2}$.

13. A method as claimed in claim 6, further comprising the step of forming diffusion regions at both lateral sides of said gate electrode pattern by introducing impurity elements into said substrate through said gate oxide film while using said gate electrode pattern as a mask, and wherein said step of introducing impurity elements is conducted prior to said step of introducing N atoms into said gate oxide film.

14. A semiconductor device, comprising:

a substrate;

a gate oxide film formed on said substrate;

a gate electrode provided on said gate oxide film;

side wall layers respectively disposed on each lateral side of said gate electrode;

first and second impurity regions respectively formed in said substrate at each lateral side of said gate electrode, which is substantially aligned the edges thereof;

first and second lightly doped impurity regions respectively formed in said substrate at each outer lateral side of said side wall layers, which is substantially aligned the edges thereof;

said gate electrode including a first region disposed right underneath said gate electrode and a second region adjacent to said first region, said first and second regions containing N atoms with

respective concentrations such that said second region contains N with a higher concentration as compared with said first region.

ABSTRACT OF THE DISCLOSURE

A semiconductor device includes a substrate, a gate oxide film formed on the substrate, a gate electrode provided on the gate oxide film, first and second diffusion regions formed in the substrate at both lateral sides of the gate electrode. The gate electrode includes a first region located immediately underneath the gate electrode and a second region adjacent to the first region, wherein the first and second regions contain N atoms with respective concentrations such that the second region contains N with a higher concentration as compared with the first region.

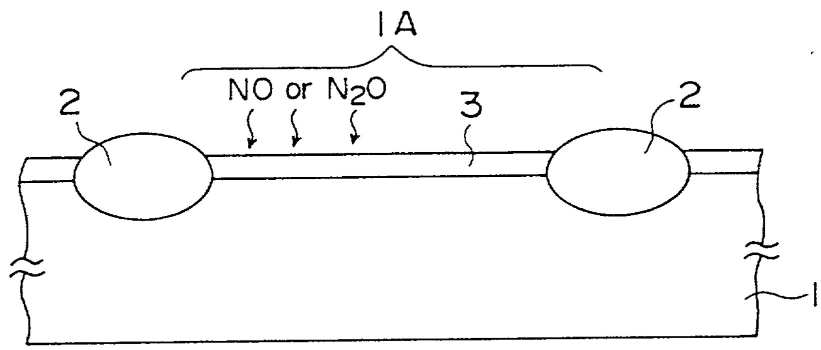


FIG. 1A
PRIOR ART

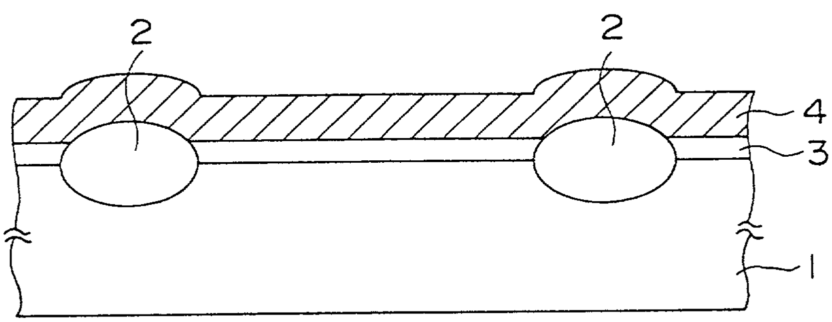


FIG. 1B
PRIOR ART

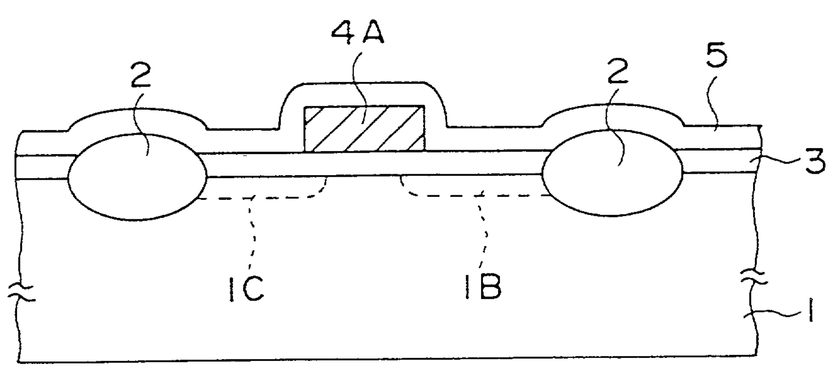


FIG. 1C
PRIOR ART

FIG. 1D
PRIOR ART

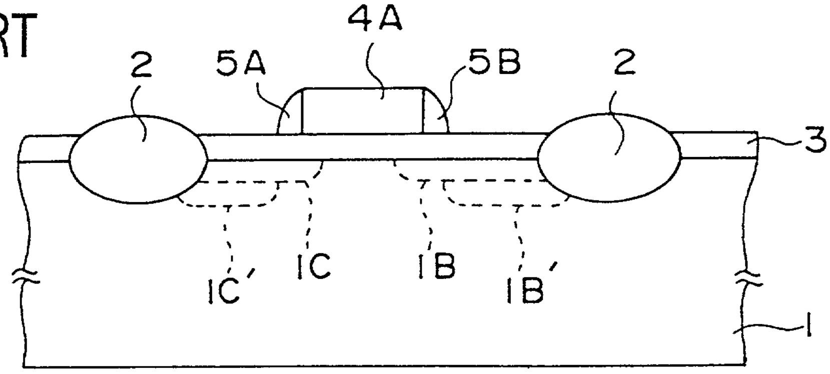


FIG. 2
PRIOR ART

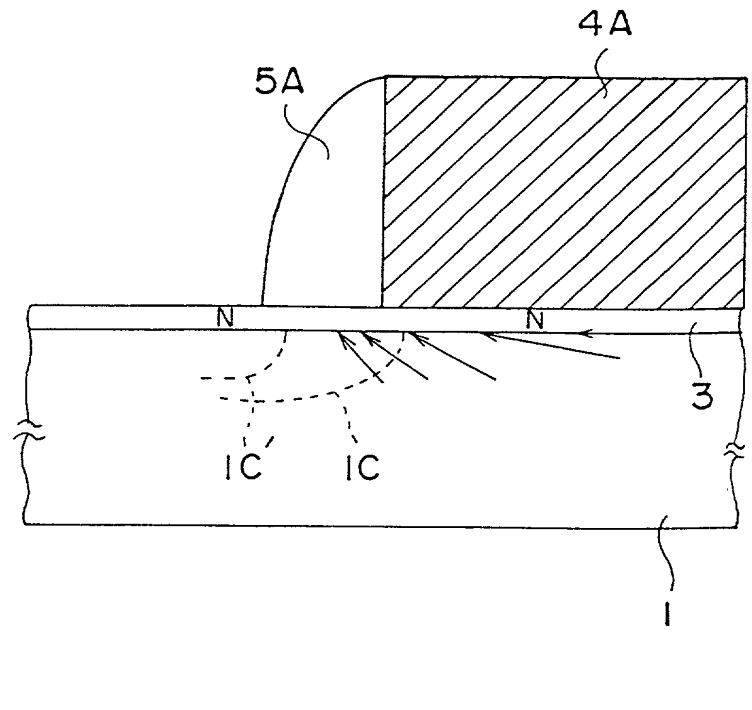


FIG. 3A PRIOR ART

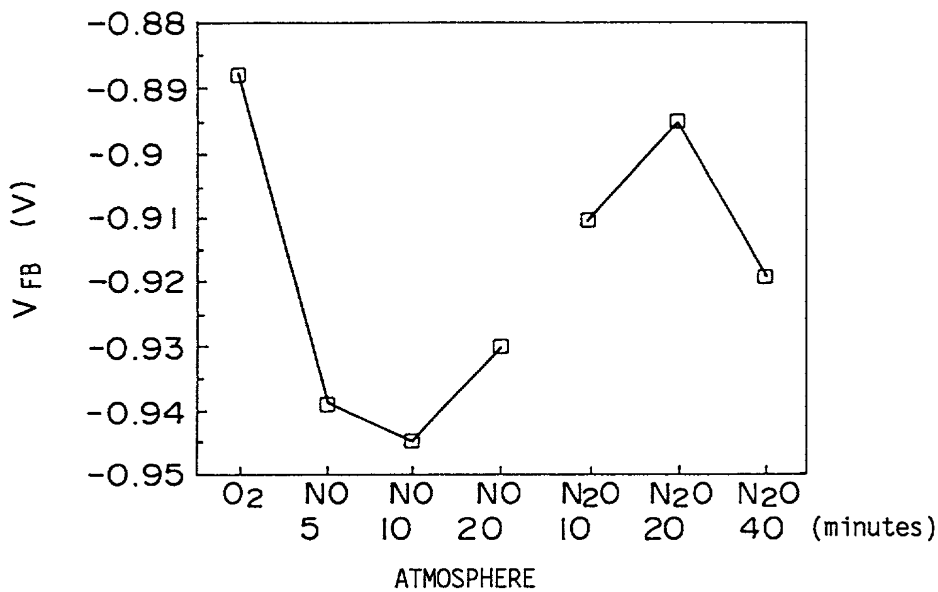


FIG. 3B PRIOR ART

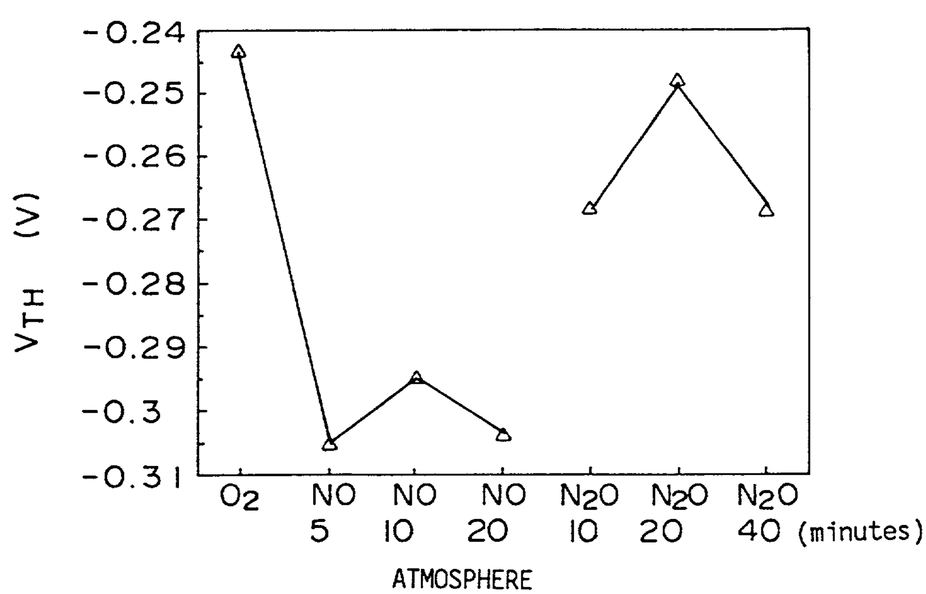


FIG. 4

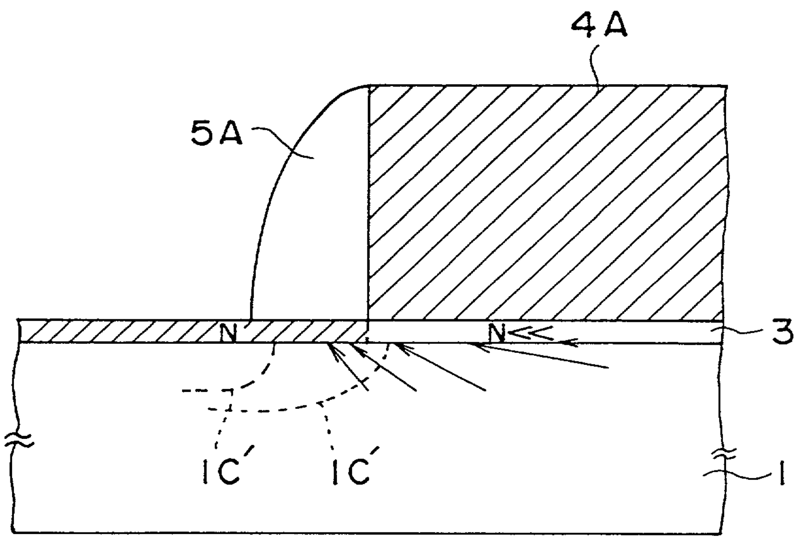


FIG. 5A

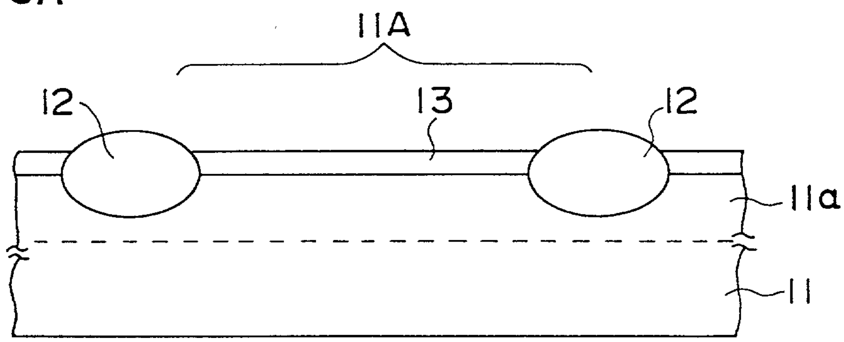


FIG. 5B

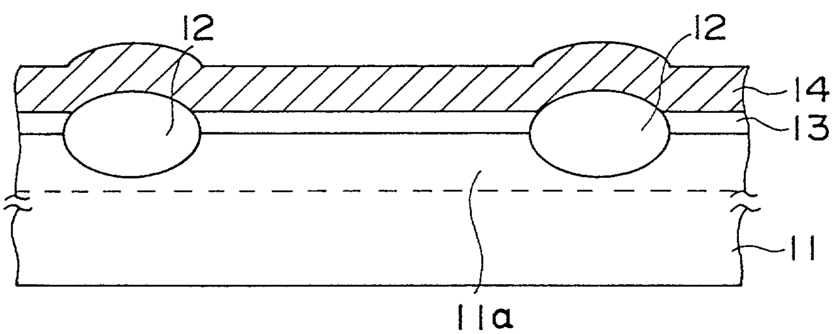


FIG. 5C

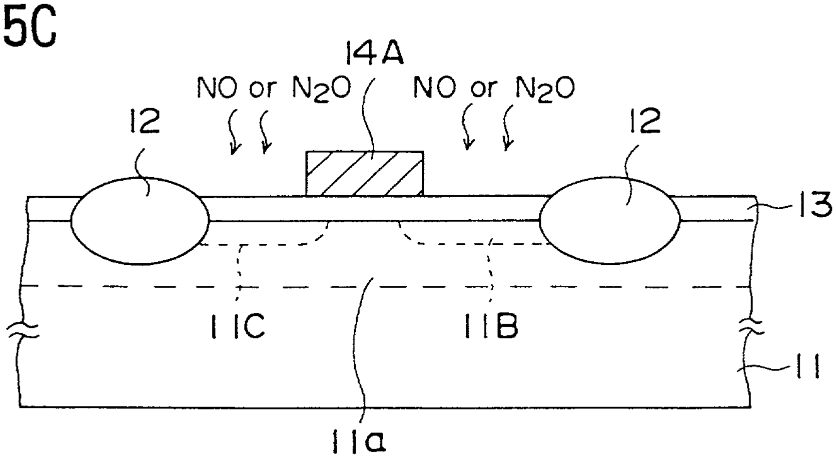


FIG. 5D

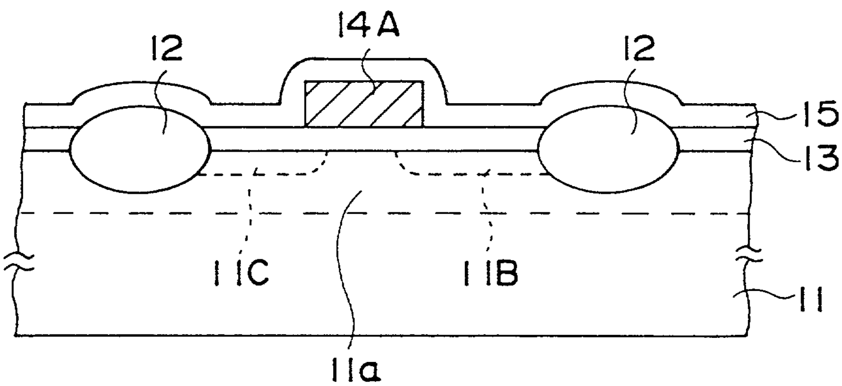

14A
12
12
15
13
11C
11B
11
11a

FIG. 5E

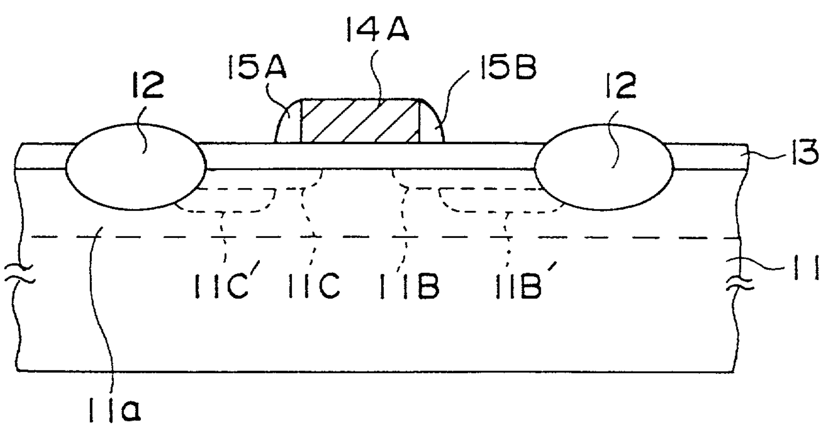

14A
15A
15B
12
12
13
11C'
11C
11B
11B'
11
11a

FIG. 5F

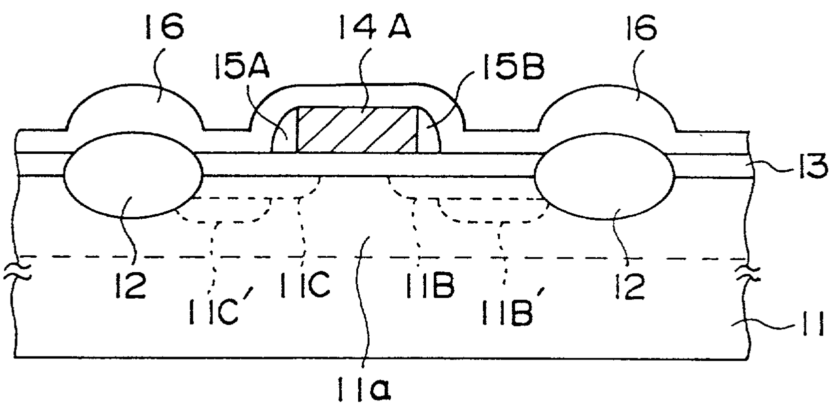

16
14A
16
15A
15B
13
12
11C
11B
12
11C'
11B'
11
11a

FIG. 5G

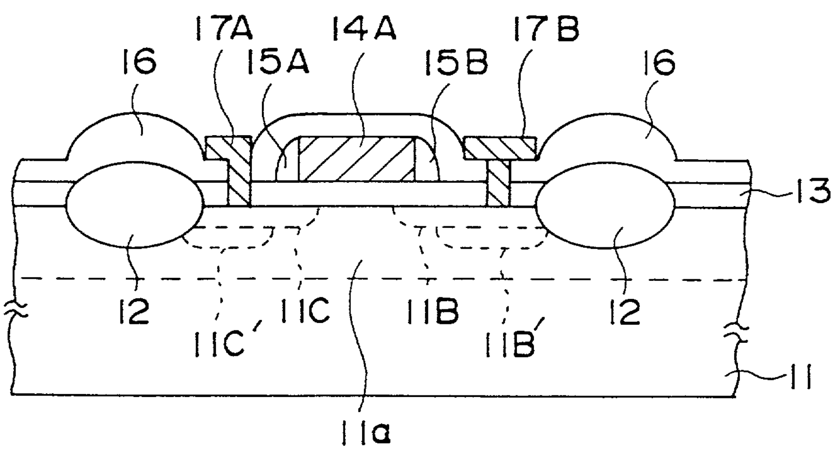

17A
14A
17B
16
15A
15B
16
13
12
11C
11B
12
11C'
11B'
11
11a

FIG. 6

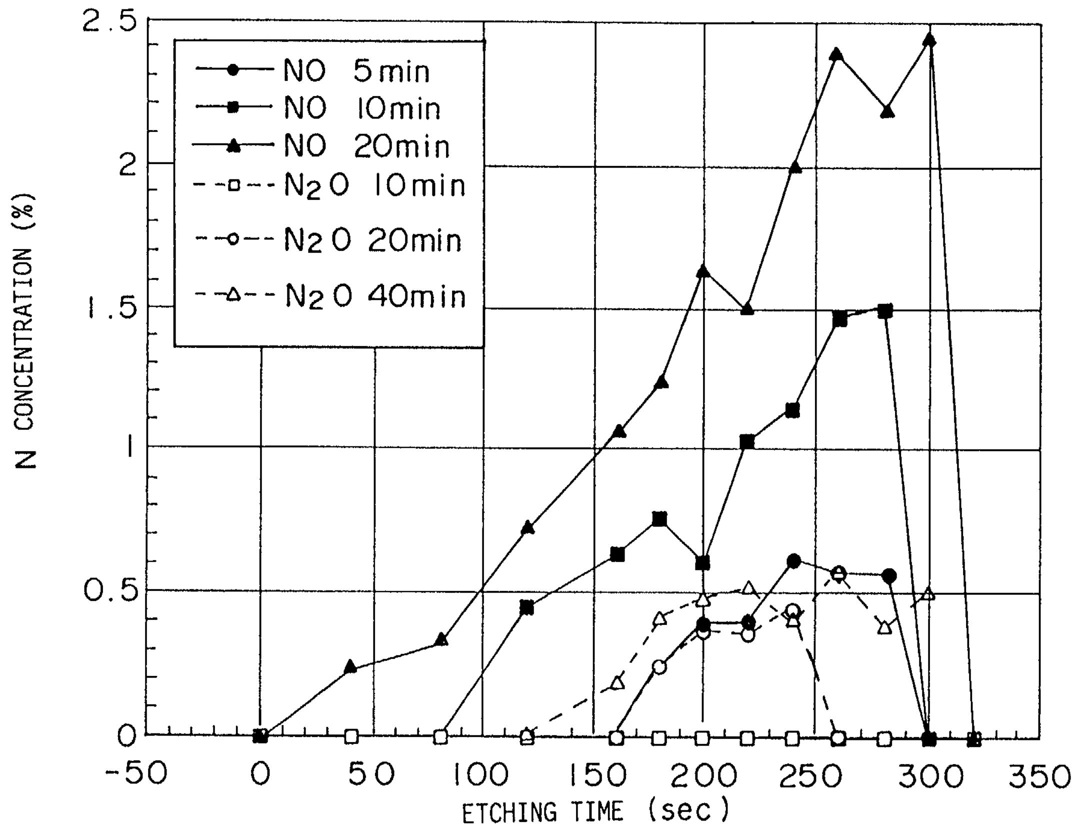

N CONCENTRATION (%)
2.5
2
1.5
1
0.5
0
-50
0
50
100
150
200
250
300
350
ETCHING TIME (sec)
NO 5min
NO 10min
NO 20min
N2O 10min
N2O 20min
N2O 40min

FIG. 7A

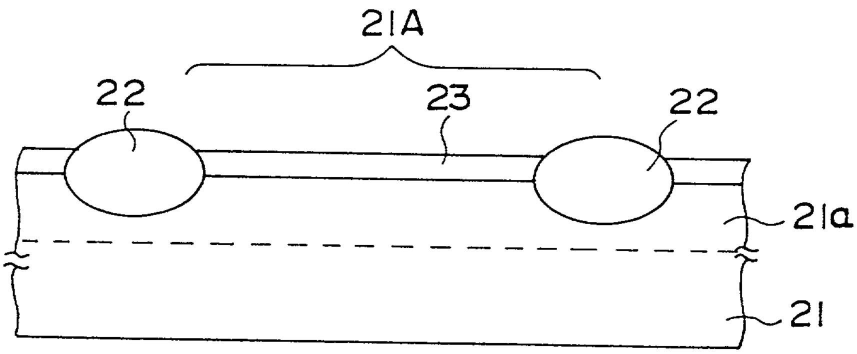


FIG. 7B

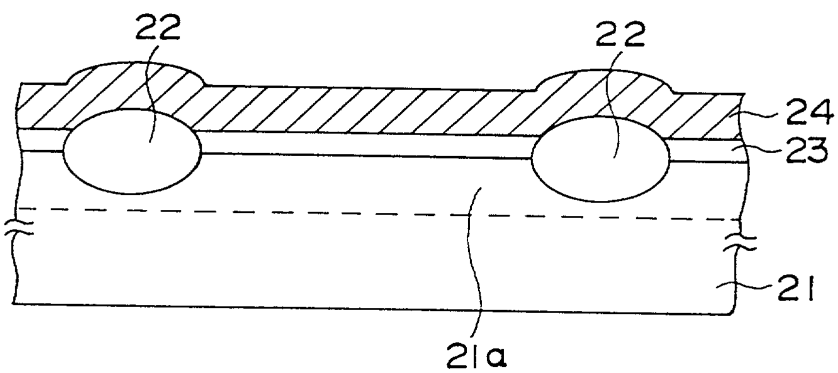


FIG. 7C

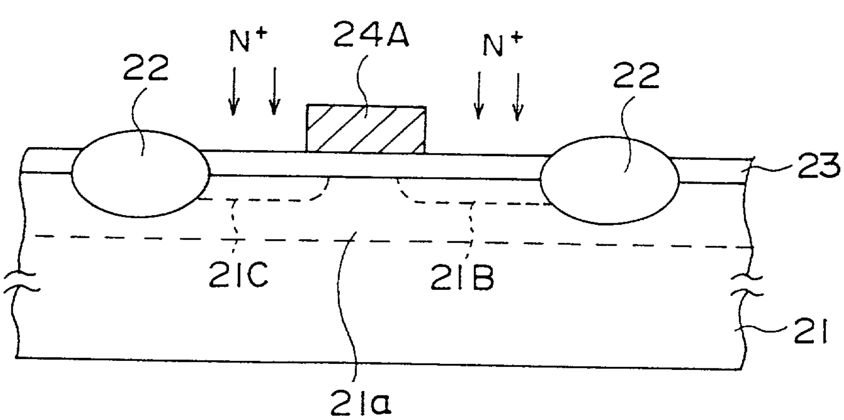


FIG. 7D

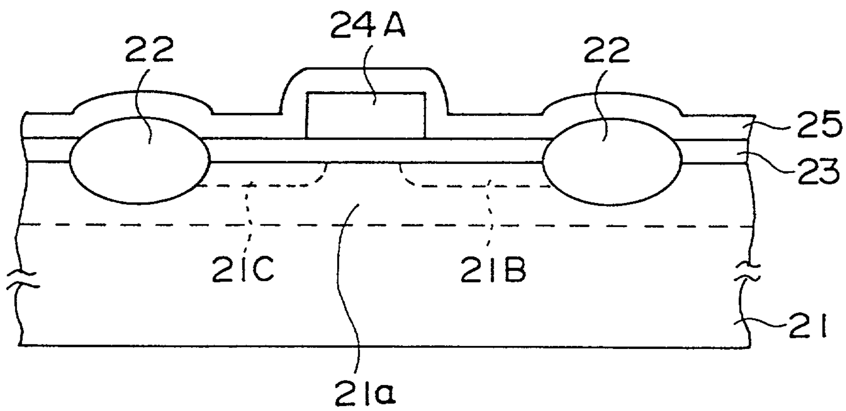

24A
22
22
25
23
21C
21B
21
21a

FIG. 7E

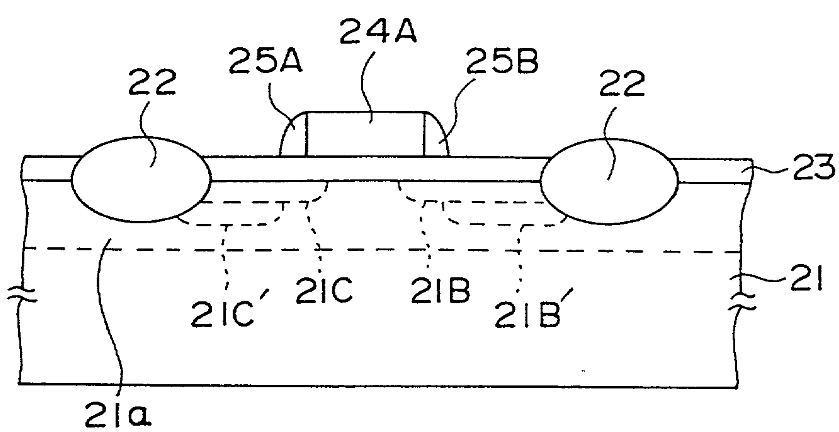

24A
25A
25B
22
22
23
21
21C′
21C
21B
21B′
21a

FIG. 7F

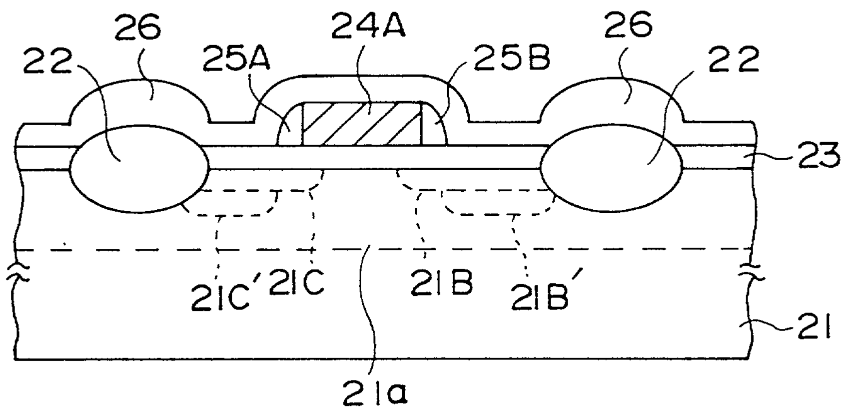

26
24A
26
22
25A
25B
22
23
21C'
21C
21B
21B'
21
21a

FIG. 7G

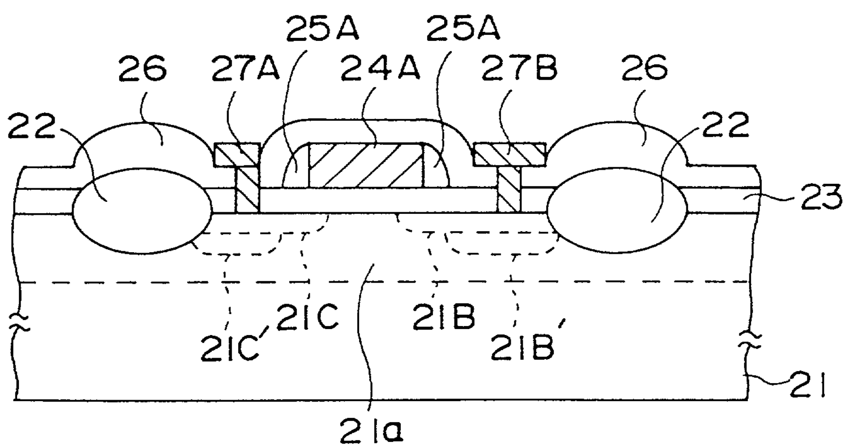
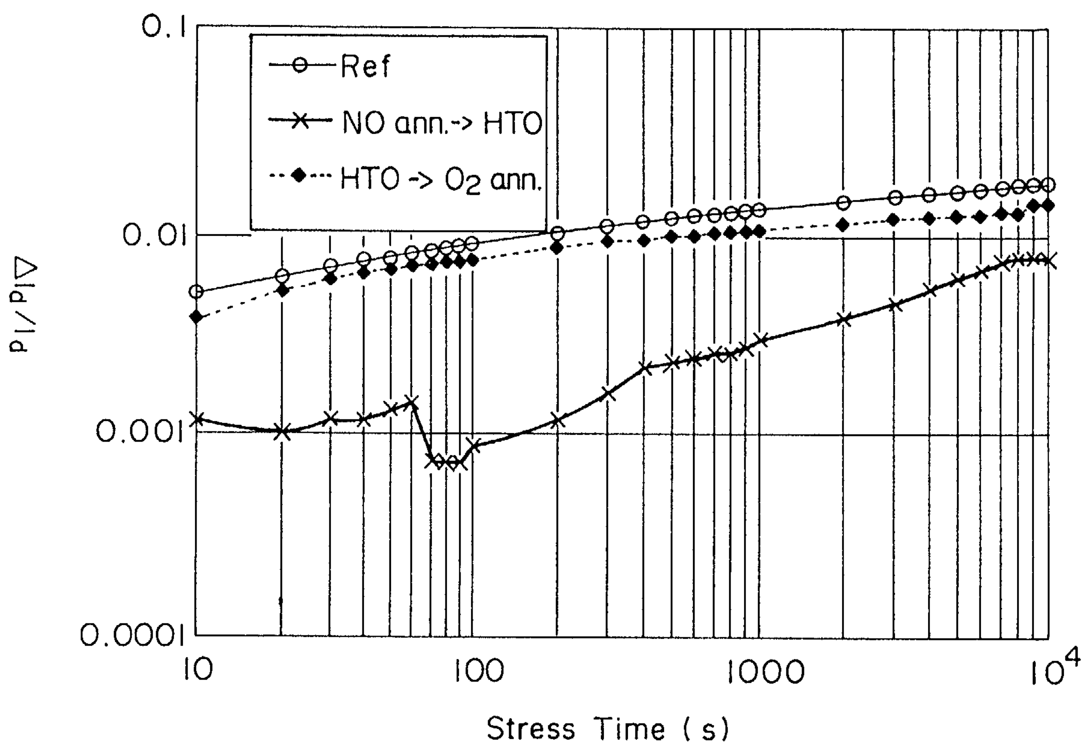

25A
25A
26
27A
24A
27B
26
22
22
23
21C
21C'
21B
21B'
21
21a

FIG. 8



Ref
NO ann.-> HTO
HTO -> O2 ann.
0.1
0.01
0.001
0.0001
$\Delta I_d / I_d$
10
100
1000
10^4
Stress Time (s)

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention **entitled** (Insert Title) SEMICONDUCTOR MEMORY DEVICE CONTAINING NITROGEN IN A GATE OXIDE FILM

the specification of which is attached hereto unless the following is checked:

☐ was filed on __________ as United States Application Number or PCT International Application Number __________ and was amended on __________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a) - (d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

(List prior foreign applications. See note A on back of this page)	(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
	Pat. Appln. No.9-052085	Japan	6/March/1997	☒ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No

(See note B on back of this page) ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of the application:

(List Prior U.S. Applications)	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

James E. Armstrong, III, Reg. No. 18,366; William F. Westerman, Reg. No. 29,988; Ken-Ichi Hattori, Reg. No. 32,861; Le-Nhung McLeland, Reg. No. 31,541; Ronald F. Naughton, Reg. No. 24,616; John R. Pegan, Reg. No. 18,069; William G. Kratz, Jr., Reg. No. 22,631; Albert Tockman, Reg. No. 19,722; Mel R. Quintos, Reg. No. 31,898; Donald W. Hanson, Reg. No. 27,133; Stephen G. Adrian, Reg. No. 32,878; William L. Brooks, Reg. No. 34,129; John F. Carney, Reg. No. 20,276; Edward F. Welsh, Reg. No. 22,455; Patrick D. Muir, Reg. No. 37,403; Gay A. Spahn, Reg. No. 34,978; and John P. Kong, Reg. No. 40,054.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(See note C above) Inventor's Signature Kiyoshi Irino Date August 7, 1997

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Full name of second inventor (given name, family name) ______

Inventor's Signature ______ Date ______

Residence ______ Citizenship ______

Post Office Address ______

Full name of third inventor (given name, family name) ______

Inventor's Signature ______ Date ______

Residence ______ Citizenship ______

Post Office Address ______

Full name of fourth inventor (given name, family name) ______

Inventor's Signature ______ Date ______

Residence ______ Citizenship ______

Post Office Address ______

Full name of fifth inventor (given name, family name) ______

Inventor's Signature ______ Date ______

Residence ______ Citizenship ______

Post Office Address ______

Full name of sixth inventor (given name, family name) ______

Inventor's Signature ______ Date ______

Residence ______ Citizenship ______

Post Office Address ______

Full name of seventh inventor (given name, family name) ______

Inventor's Signature ______ Date ______

Residence ______ Citizenship ______

Post Office Address ______

Full name of eighth inventor (given name, family name) ______

Inventor's Signature ______ Date ______

Residence ______ Citizenship ______

Post Office Address ______